In the Claims:

There are no revisions to the claims.

1. (Original) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising the steps of:

providing a substrate having a gate structure formed thereon;

forming a dielectric spacer layer over the semiconductor substrate; and

etching said dielectric spacer layer, prior to forming a layer subsequent to the dielectric layer, to form L-shaped spacers.

2. (Previously Amended) The method of Claim 1, further including the step of forming a liner oxide layer over said gate structure prior to the step of forming the dielectric spacer layer.

3. (Previously Amended) The method of Claim 2 wherein said liner oxide layer is deposited to a thickness of between approximately 20 Angstroms and 200 Angstroms.

4. (Previously Amended) The method of Claim 1 wherein said dielectric spacer layer comprises a nitride layer.

5. (Previously Amended) The method of Claim 3, wherein the said dielectric spacer has a thickness in the range of 150 Angstroms and 500 Angstroms.

6. (Previously Amended) The method of Claim 1 wherein said dielectric spacer layer comprises a silicon oxynitride layer.

7. (Previously Amended) The method of Claim 1 wherein the step of etching said dielectric layer includes anisotropically etching said dielectric layer to form L-shaped spacers, said L-shaped spacers having vertical portions varying in thickness and horizontal portions varying in thickness.

8. (Previously Amended) The method of Claim 7, wherein said and horizontal portion of the L-shaped spacers having bulging profiles varying gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthers from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.

9. (Previously Amended) The method of Claim 7 wherein said dielectric layer is anisotropically etched using a capacitively coupled plasma etch process with an etching chemistry comprising CH3F and O2 in combination with an inert gas to form said L-shaped spacers.

10. (Previously Amended) The method of Claim 7, wherein said dielectric layer is anisotropically etched using an inductively coupled plasma etch process with an etching chemistry comprising CH3F and O2 in combination with an inert gas.

11. (Previously Amended) The method of Claim 1, wherein the step of etching said dielectric layer to form said L-shaped spacers includes using CH3F and O2 chemistry in ratios ranging from approximately 2:1 to approximately 5:1 CH3F to O2.

12. (Previously Amended) The method of Claim 11, wherein the step of etching said dielectric layer to form said L-shaped spacers utilizes a pressure during the etch process ranging from approximately 20 milliTorr to approximately 500 milliTorr.

13. (Previously Amended) The method of Claim 11, wherein the step of etching includes using a temperature ranging from approximately 10 degrees C and 30 degrees C.

14. (Withdrawn)

15. (Withdrawn)

16. (Withdrawn)

17. (Withdrawn)

18. (Original) A method for fabricating sidewall spacers in the manufacture of an integrated circuit device, comprising the steps of:

providing a substrate having a gate structure formed thereon;

forming a liner oxide layer on said gate structure;

forming a dielectric spacer layer over said liner oxide layer; and

anisotropically etching said dielectric layer, prior to forming a layer subsequent to the dielectric layer, to form L-shaped spacers, said L-shaped spacers having vertical portions and a horizontal portion, wherein the horizontal portion varies gradually in thickness from a maximum thickness immediately adjacent the vertical portion of the L-shaped spacer to a portion of the L-shaped spacer furthest from the vertical-portion of the L-shaped spacer, wherein the horizontal portion varies gradually to provide for an average thickness of the L-shaped portion that is 50 to 85 percent of the maximum thickness.